P-Channel Enhancement Mode MOSFET

1. Product Information

1.1 Features

- ☑ Advanced trench cell design
- ☑ Low Thermal Resistance

1.2 Applications

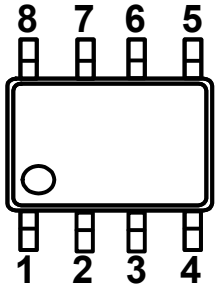
- ☑ Motor drivers
- ☑ DC - DC Converter

1.3 Quick reference

- ☑ BV ≧ -30 V
- ☑ P_{tot} ≦ 2 W
- ☑ I_D ≦ -15A
- ☑ $R_{DS(ON)}$ ≦ 9.5 mΩ @ V_{GS} = - 10 V
- ☑ $R_{DS(ON)}$ ≦ 14 mΩ @ V_{GS} = - 4.5 V

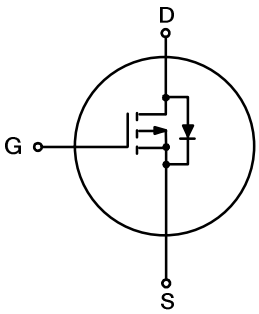
2. Pin Description

Pin	Description
1,2,3	Source(S)
4	Gate(G)
5,6,7,8	Drain(D)



Top View

SOP-8L



3. Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	T_C = 25 ℃	-	-30	V
V_{GS}	Gate-Source Voltage	T_C = 25 ℃	-	± 20	V
I_D*	Drain Current	T_C = 25 ℃, V_{GS} = -10 V	-	-15	A
I_{DM}*,**,***	Pulsed Source Current	T_C = 25 ℃, V_{GS} = -10 V	-	-40	A
P_{tot}*	Total Power Dissipation	T_C = 25 ℃	-	2	W
T_{stg}	Storage Temperature		- 55	150	℃
T_J	Junction Temperature		-	150	℃
I_S	Diode Forward Current	T_C = 25 ℃	-	-15	A
$R_{\theta JC}$*	Thermal Resistance- Junction to Ambient		-	6	℃ / W

Notes：

* Surface Mounted on 1 in^2 pad area, $t \leq 10$ sec

** Pulse width ≤ 10 μs, duty cycle ≤ 1 %

*** Limited by bonding wire

4. Marking Information

Product Name	Marking
N4407S	**4407** **YWWXXX** **YWWXXX: Date Code**

5. Ordering Code

Product Name	Package	Reel Size	Tape width	Quantity	Note
N4407S	**SOP8**			**3000**	

6. Electrical Characteristics (T_C = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = -250 μA	-1.0	-	-2.0	V
I_{DSS}	Zero Gate Voltage Source Current	V_{DS} = -24 V, V_{GS} = 0 V	-	-	-1	μA
		T_J = 85 ℃	-	-	-30	μA
I_{GSS}	Gate Leakage Current	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	± 100	nA
$R_{DS(ON)}$[a]	Drain-Source On-State Resistance	V_{GS} = -10 V, I_D = - 8A	-	8.5	9.5	mΩ
		V_{GS} = -4.5 V, I_D = -5 A	-	11.5	14	mΩ
Diode Characteristics						
V_{SD}[a]	Diode Forward Voltage	I_{SD} = -12 A, V_{GS} = 0 V	-	-	-1.3	V
t_{rr}	Reverse Recovery Time	I_{SD} = -12 A, dI_{SD}/dt = 100 A/μs	-	8.3	-	nS
Q_{rr}	Reverse Recovery Charge		-	0.6	-	nC
Dynamic Characteristics[b]						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = -15 V Frequency = 1 MHz	-	2215	-	pF
C_{oss}	Output Capacitance		-	310	-	
C_{rss}	Reverse Transfer Capacitance		-	237	-	
t_d(on)	Turn-on Delay Time	V_{DS} = -15 V, V_{GEN} = -10 V, R_G = 4.5 Ω, R_L = 0.75 Ω, I_D = -12 A	-	33	-	nS
t_r	Turn-on Rise Time		-	35	-	
t_d(off)	Turn-off Delay Time		-	72	-	
t_f	Turn-off Fall Time		-	10	-	
Gate Charge Characteristics[b]						
Q_g	Total Gate Charge	V_{GS} = -10 V, V_{DS} = -15 V, I_{DS} = -12 A	-	20	-	nC
Q_{gs}	Gate-Source Charge		-	5.1	-	
Q_{gd}	Gate-Drain Charge		-	7.3	-	

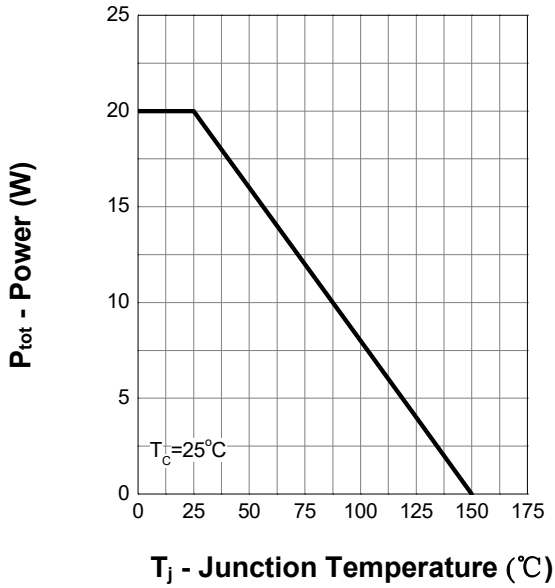
Notes：

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2 %

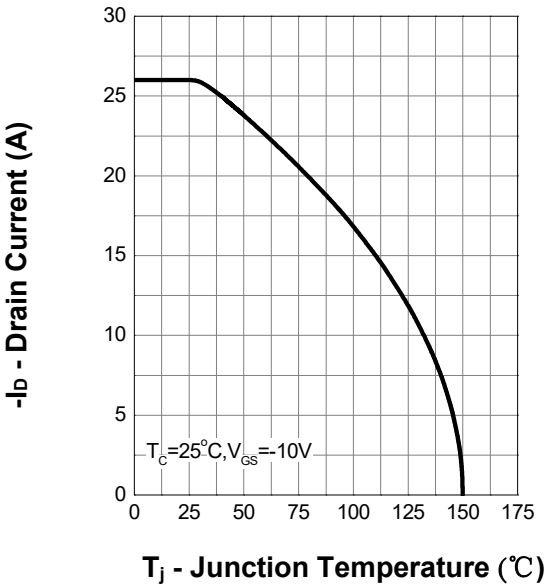
b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

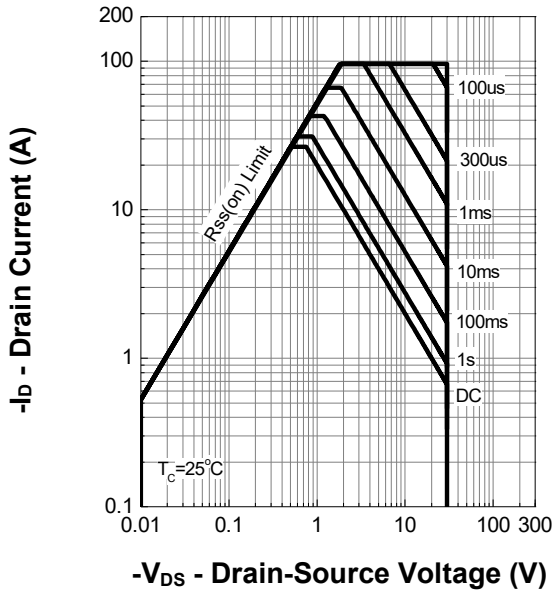
Power Capability



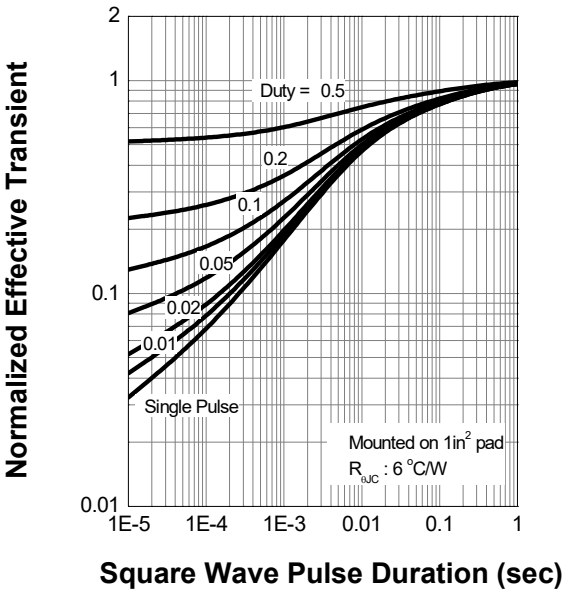
Current Capability



Safe Operation Area

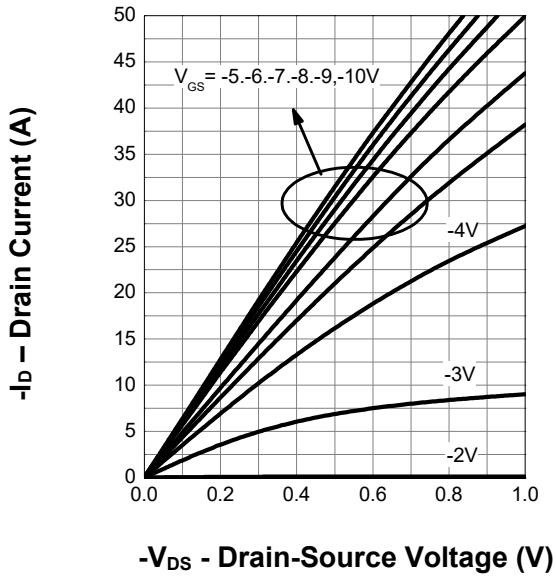


Thermal Transient Impedance

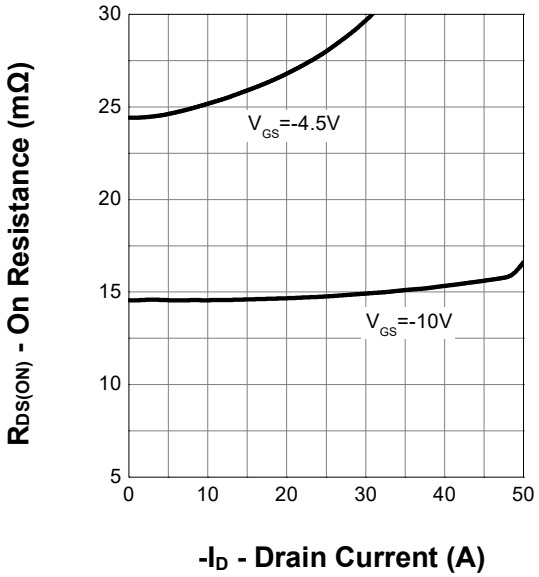


7. ypical Characteristics (cont.)

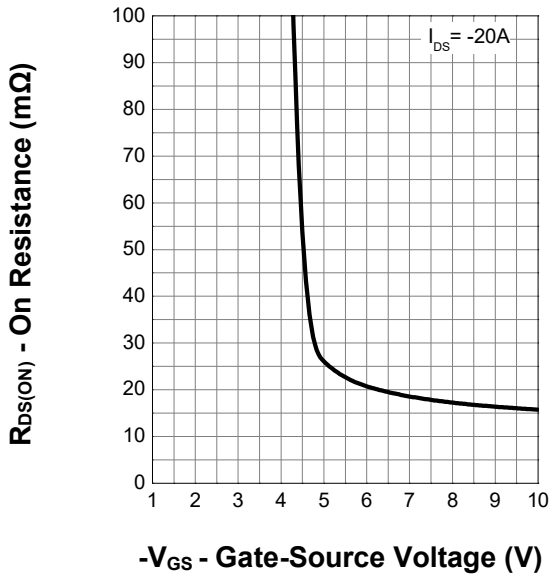
Output Characteristics



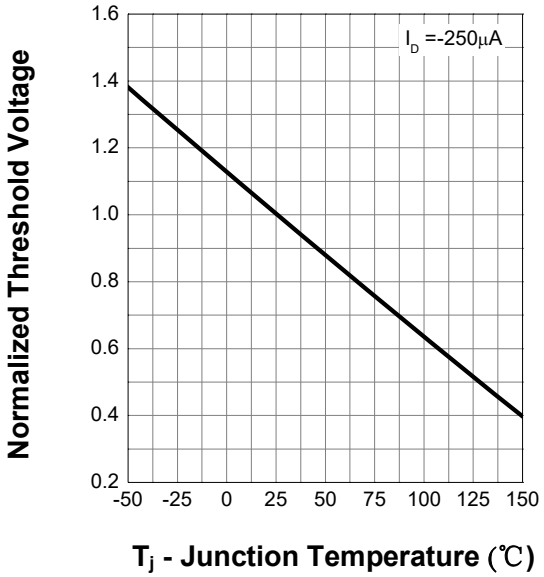
Drain-Source On Resistance



Transfer Characteristics

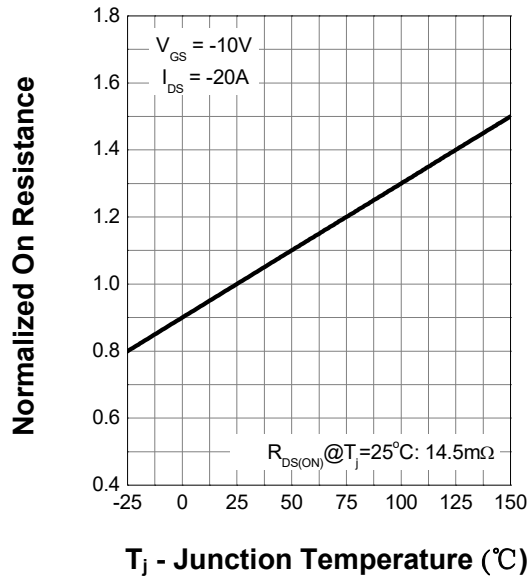


Gate Threshold Voltage

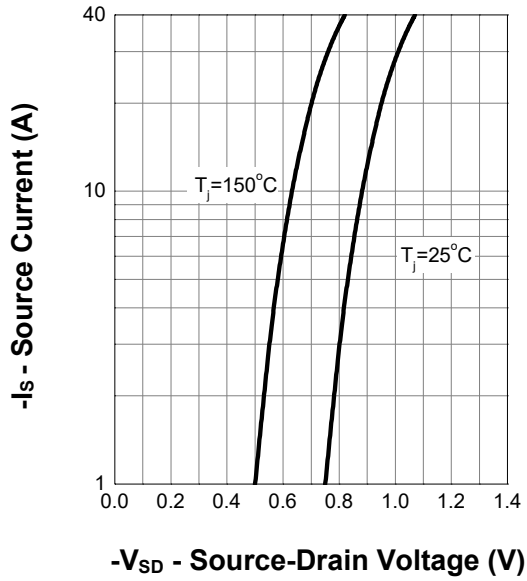


7. ypical Characteristics (cont.)

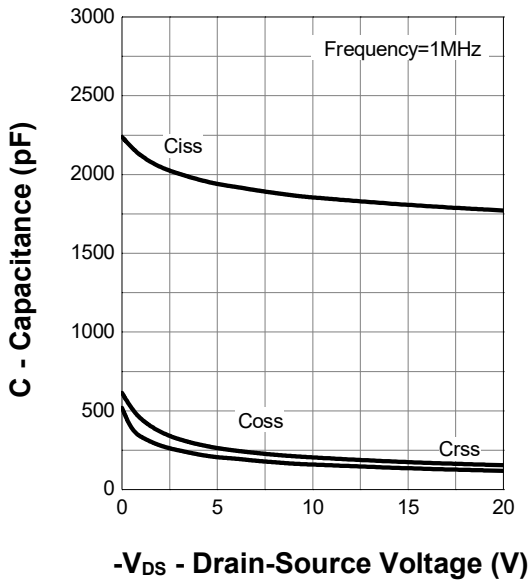
Drain-Source On Resistance



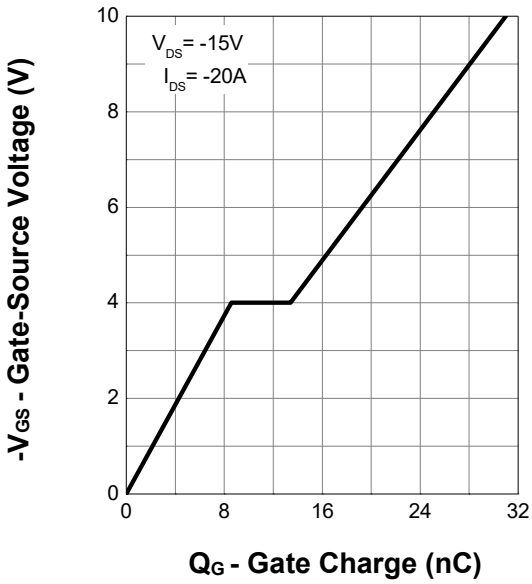
Body Diode Characteristics



Capacitance



Gate Charge



8. Package Dimensions

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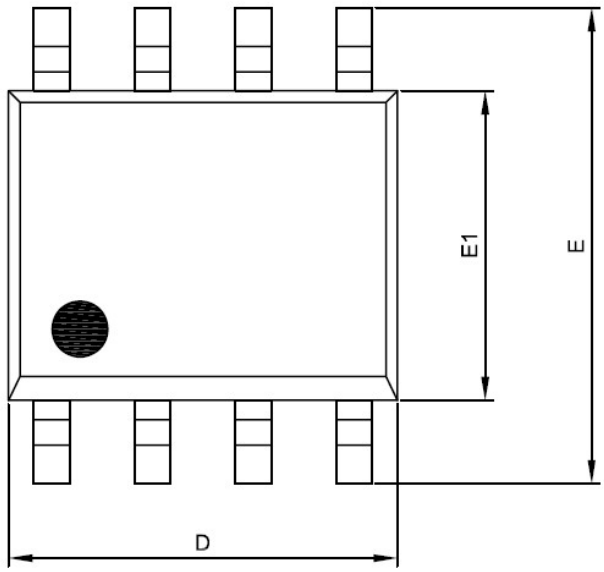

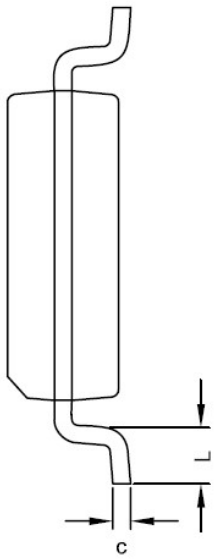

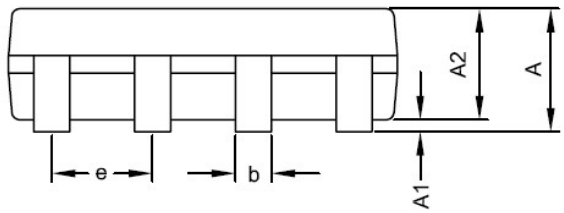

Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.