# Dual N-Channel Enhancement Mode MOSFET

## 1. Product Information

### 1.1 Features

- ☑ Surface-mounted package
- ☑ Advanced trench cell design

### 1.2 Applications

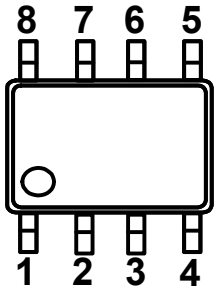
- ☑ LCD TV appliances
- ☑ LCDM appliances
- ☑ High power inverter system

### 1.3 Quick reference

- ☑ BV ≧ 60 V
- ☑ $P_{tot}$ ≦ 2 W
- ☑ $I_D$ ≦ 8 A
- ☑ $R_{DS(ON)}$ ≦ 32mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ ≦ 38mΩ @ $V_{GS}$ = 4.5V

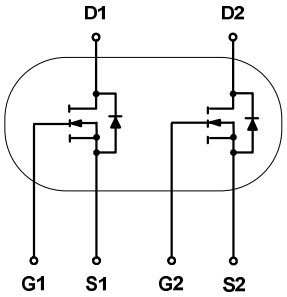
## 2. Pin Description

| Pin | Description | Simplified Outline | Symbol |
|---|---|---|---|
| 1 | Source(S1) | | |
| 2 | Gate(G1) | | |
| 3 | Source(S2) | | |
| 4 | Gate(G2) | | |
| 5,6 | Drain(D2) | | |
| 7,8 | Drain(D1) | | |




Top View

SOP- 8L



## 3. Limiting Values

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | $T_A$ = 25 ℃ | - | 60 | V |
| $V_{GS}$ | Gate-Source Voltage | $T_A$ = 25 ℃ | - | ± 20 | V |
| $I_D$* | Drain Current | $T_A$ = 25 ℃, $V_{GS}$ = 10 V | - | 8 | A |
| | | $T_A$ = 100 ℃, $V_{GS}$ = 10 V | - | 3.9 | A |
| $I_{DM}$*,** | Pulsed Drain Current | $T_A$ = 25 ℃, $V_{GS}$ = 10 V | - | 24.8 | A |
| $P_{tot}$ | Total Power Dissipation | $T_A$ = 25 ℃ | - | 2 | W |
| $T_{stg}$ | Storage Temperature | | - 55 | 150 | ℃ |
| $T_J$ | Junction Temperature | | - 55 | 150 | ℃ |
| $I_S$ | Diode Forward Current | $T_A$ = 25 ℃ | - | 8 | A |
| $R_{\theta JA}$* | Thermal Resistance- Junction to Ambient | | - | 56 | ℃ / W |

Notes :

* Surface Mounted on 1 $in^2$ pad area, t ≤ 10 sec

** Pulse width ≤ 300 μs, duty cycle ≤ 2 %

## 4. Marking Information

| Product Name | Marking |
|---|---|
| **N4946S** | **4946**<br>**YWWXXX**<br>**YWW: Date Code** |

## 5. Ordering Code

| Product Name | Package | Reel Size | Tape width | Quantity | Note |
|---|---|---|---|---|---|
| **N4946S** | **SOP-8L** | | | **3000** | |

## 6. Electrical Characteristics ( $T_A$=25 °C Unless Otherwise Noted )

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Static Characteristics | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 250 μA | 60 | - | - | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 μA | 1.0 | - | 2.0 | V |
| $I_{DSS}$ | Drain Leakage Current | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $T_J$ = 85 ℃ | - | - | 30 | μA |
| $I_{GSS}$ | Gate Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | - | - | ± 100 | nA |
| $R_{DS(ON)}$[a] | On-State Resistance | $V_{GS}$ = 10 V, $I_{DS}$ = 6 A | - | 27 | 32 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_{DS}$ = 3 A | - | 34 | 38 | |
| Diode Characteristics | | | | | | |
| $V_{SD}$[a] | Diode Forward Voltage | $I_{SD}$ = 6 A , $V_{GS}$ = 0V | - | - | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = 6 A , $dI_{SD}/dt$ = 100 A/μs | - | 12.2 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 2.2 | - | nC |
| Dynamic Characteristics[b] | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V<br>Frequency = 1 MHz | - | 1051 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 42 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 35 | - | |
| $t_d$(on) | Turn-on Delay Time | $V_{DS}$ = 30 V, $V_{GEN}$ = 10 V,<br>$R_G$ = 4.5 Ω, $R_L$ = 5 Ω,<br>$I_{DS}$ = 6 A | - | 7.4 | - | ns |
| $t_r$ | Turn-on Rise Time | | - | 26 | - | |
| $t_d$(off) | Turn-off Delay Time | | - | 17.6 | - | |
| $t_f$ | Turn-off Fall Time | | - | 28 | - | |
| Gate Charge Characteristics[b] | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 10 V, $V_{DS}$ = 30 V,<br>$I_{DS}$ = 6 A | - | 19.5 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 5.4 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 2.6 | - | |

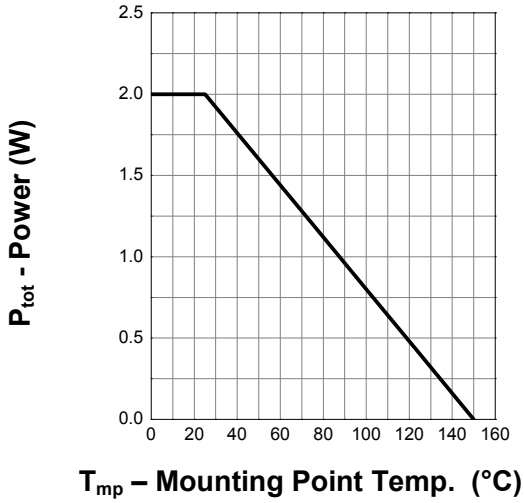
Notes：

a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%

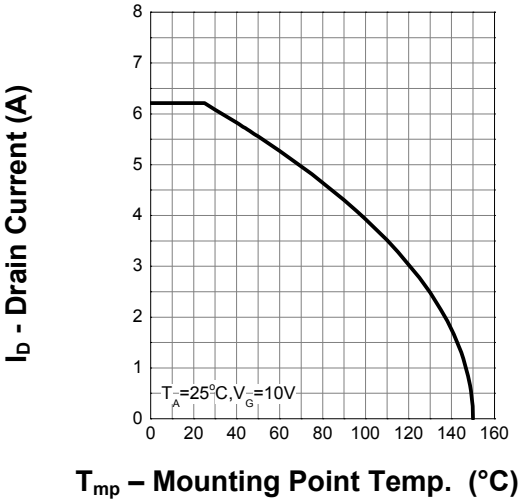
b : Guaranteed by design, not subject to production testing

## 7. Typical Characteristics

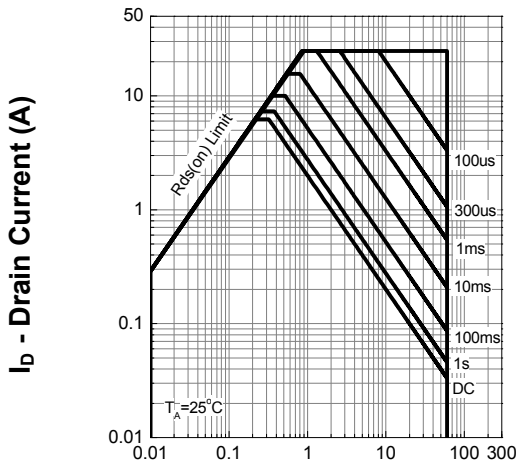
**Power Capability**



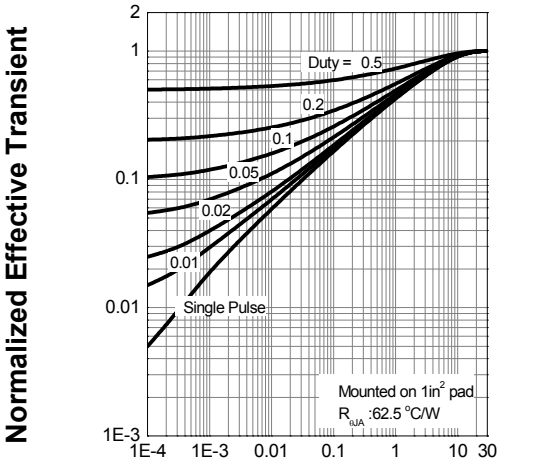

**Current Capability**




**Operating**

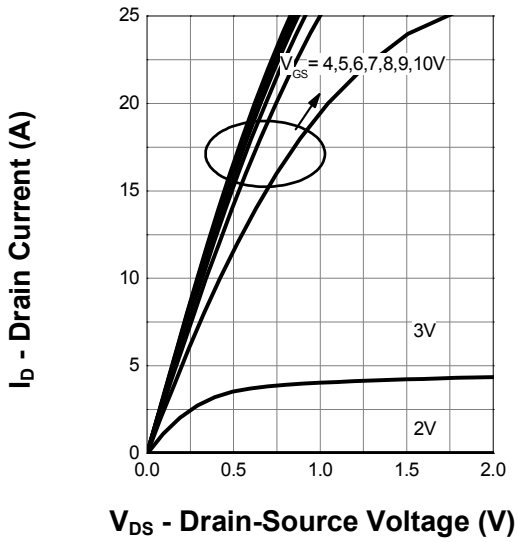



**Transient Thermal Impedance**

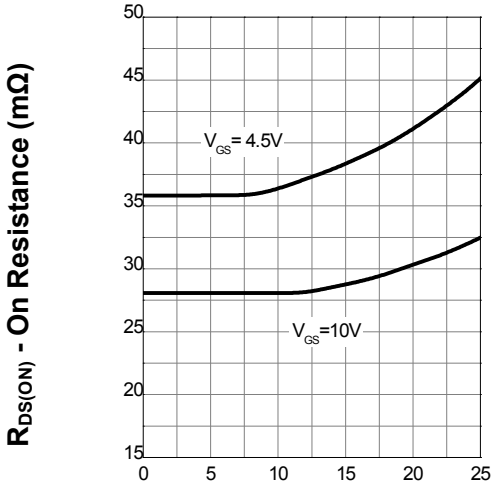


## 7. Typical Characteristics (cont.)

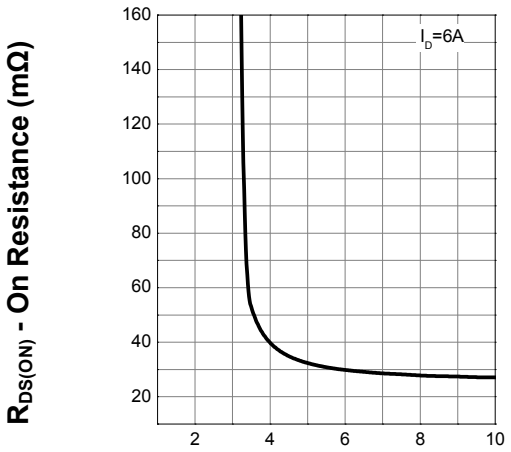
**Output Characteristics**



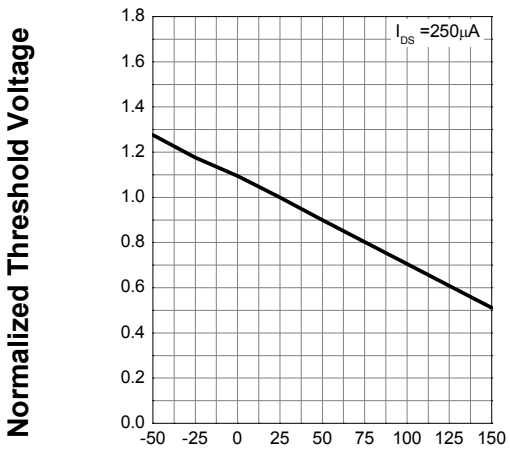

**On Resistance**




**Transfer Characteristics**

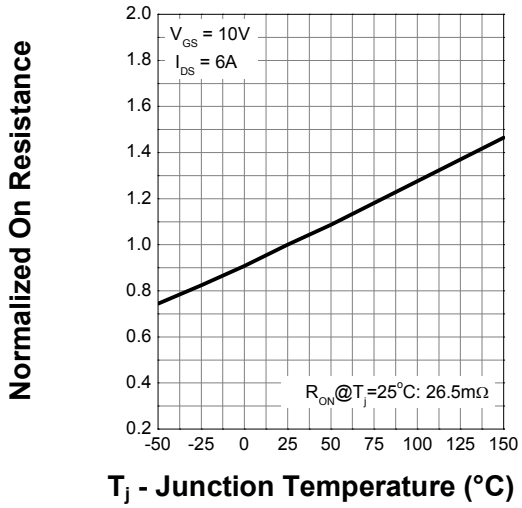



**Normalized Threshold Voltage**

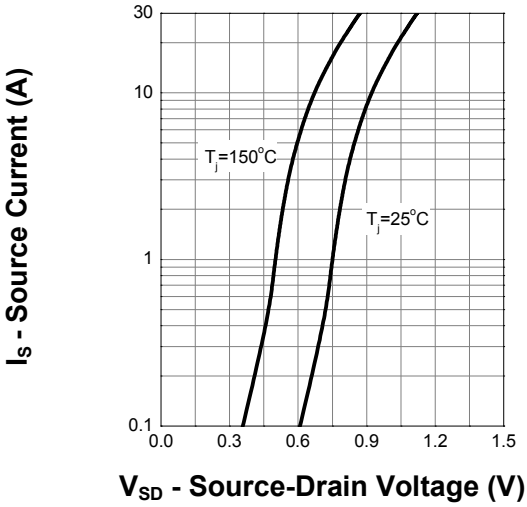


# 7. Typical Characteristics (cont.)

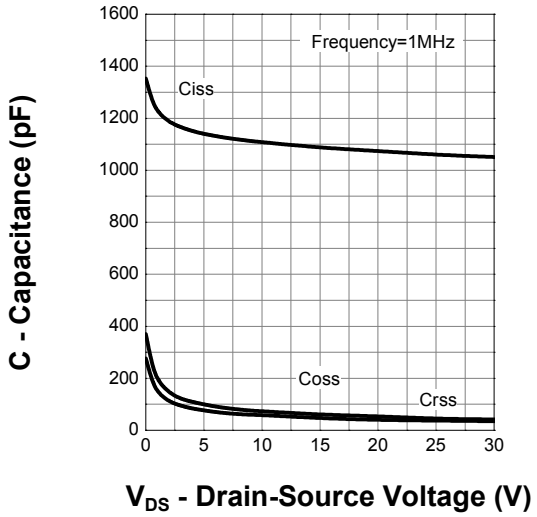
**Normalized On Resistance**



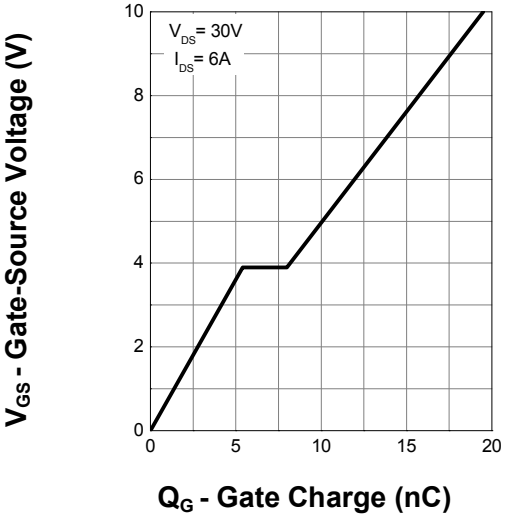

**Diode Forward Current**




**Capacitance**

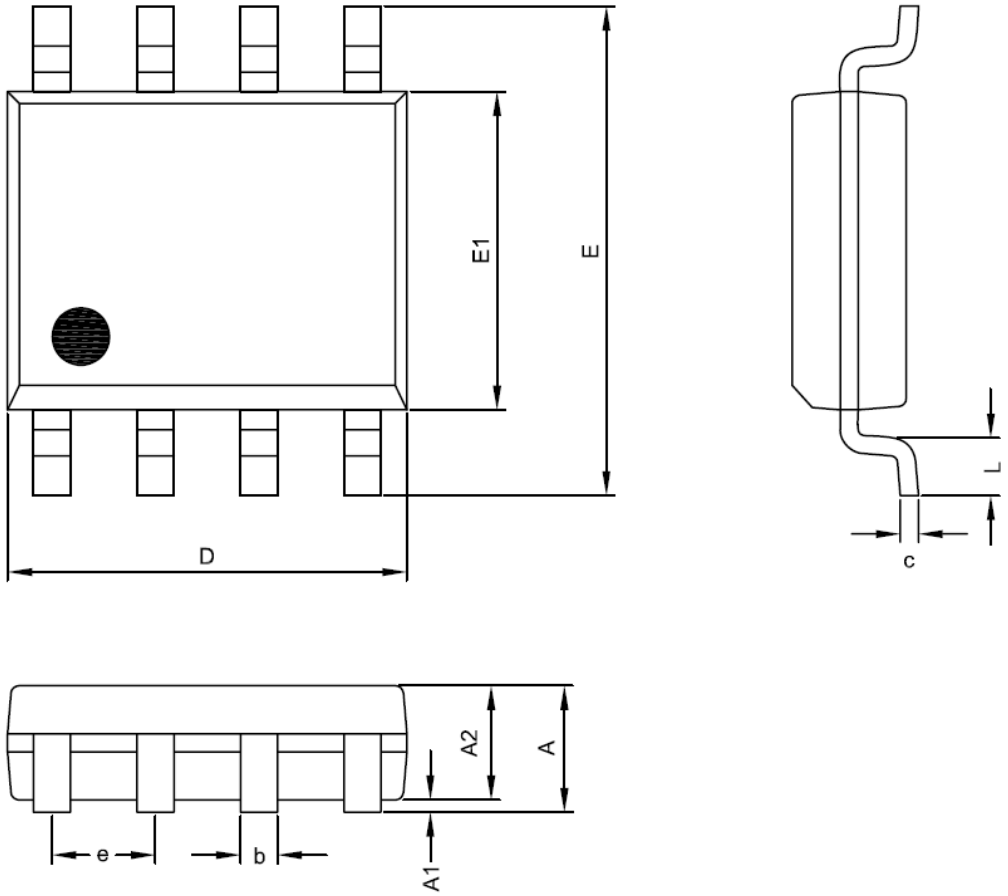



**Gate Charge**



# 8. Package Dimensions

**SOP- 8L**




| Symbol | Dimensions In Millimeters | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.35 | 1.75 |
| A1 | 0.00 | 0.25 |
| A2 | 1.15 | 1.50 |
| D | 4.80 | 5.00 |
| E | 5.80 | 6.20 |
| E1 | 3.80 | 4.00 |
| c | 0.19 | 0.27 |
| b | 0.33 | 0.53 |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.