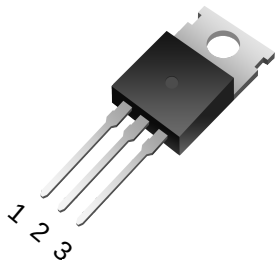
TO-220-3L Plastic-Encapsulate MOSFETS

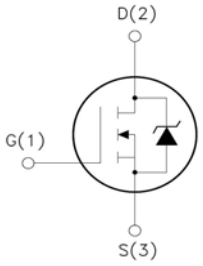
100V N-Channel Power SGT MOSFET

FEATURE

- Advanced Trench Technology
- Excellent Switching Characteristics
- Extended Safe Operating Area
- Ultra Low Gate Charge:Qg=82nC (Typ.)
- VDSS=100V, ID=130A
- Rds(on):4.4mΩ(Typ.) @VG=10V
- 100% Avalanche Tested

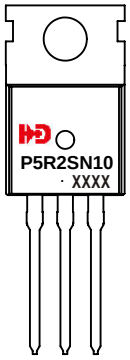
TO-220-3L





1.Gate (G)
2.Drain (D)
3.Source (S)

MARKING



P5R2SN10 Device code.
Solid dot = Green molding compound device, if none, the normal device.
XXXX = Code.

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	100	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (1)	T_C = 25°C	I_D	130	A
	T_C = 100°C		86	
Pulsed Drain Current (2)		I_{DM}	572	A
Avalanche Energy (3)		E_{AS}	590	mJ
Power Dissipation (4)	T_C = 25°C	P_D	192	W
	T_C = 100°C		76	
Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Performance

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	45	55	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.40	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_a=25℃ unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250μA, V_{GS} = 0V	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1.0	μA
		T_J = 55°C			5.0	
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.3	4.5	V
Static Drain-Source ON-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 65A		4.4	5.2	mΩ
		V_{GS} = 10V, I_D = 30A		5.2	7.0	
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 20A		44		S
Diode Forward Voltage	V_{SD}	I_S = 1A, V_{GS} = 0V		0.66	1.0	V
Diode Continuous Current	I_S	T_C = 25°C			143	A
DYNAMIC PARAMETERS (5)						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		4335		pF
Output Capacitance	C_{oss}			678		pF
Reverse Transfer Capacitance	C_{rss}			20.9		pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS}= 0V, f = 1MHz		2.0		Ω
SWITCHING PARAMETERS (5)						
Total Gate Charge (@ V_{GS} = 10V)	Q_g	V_{GS} = 0 to 10V V_{DS} = 50V, I_D = 20A		82		nC
Total Gate Charge (@ V_{GS} = 6.0V)	Q_g			41		nC
Gate Source Charge	Q_{gs}			23		nC
Gate Drain Charge	Q_{gd}			13.9		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS} = 10V, V_{DS} = 50V R_L = 2.5Ω, R_{GEN} = 3Ω		16.7		ns
Turn-On Rise Time	t_r			21		ns
Turn-Off DelayTime	$t_{D(off)}$			37		ns
Turn-Off Fall Time	t_f			15.6		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F = 65A, dI_F/dt = 100A/μS		57		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F = 65A, dI_F/dt = 100A/μS		110		nC

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under T_{J_Max} = 150°C.
3. E_{AS} of 590 mJ is based on starting T_J = 25°C, L = 3.0mH, I_{AS} = 20A, V_{GS} = 10V, V_{DD} = 50V; 100% test at L = 0.1mH, I_{AS} =48A.
4. The power dissipation P_D is based on T_{J_Max} = 150°C.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

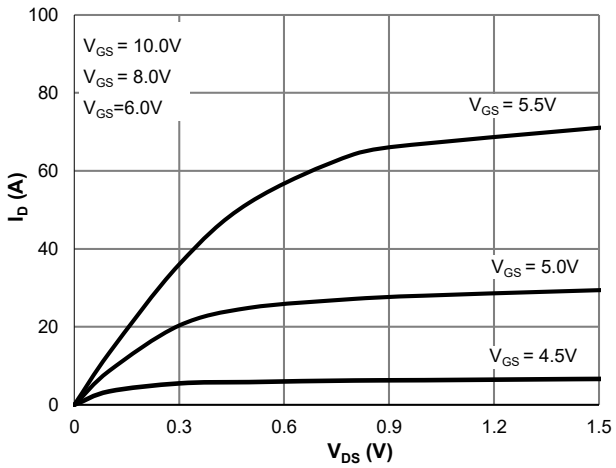


Figure 1: Saturation Characteristics

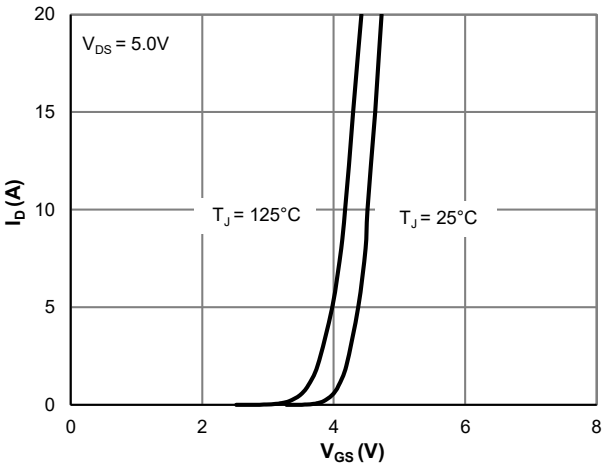


Figure 2: Transfer Characteristics

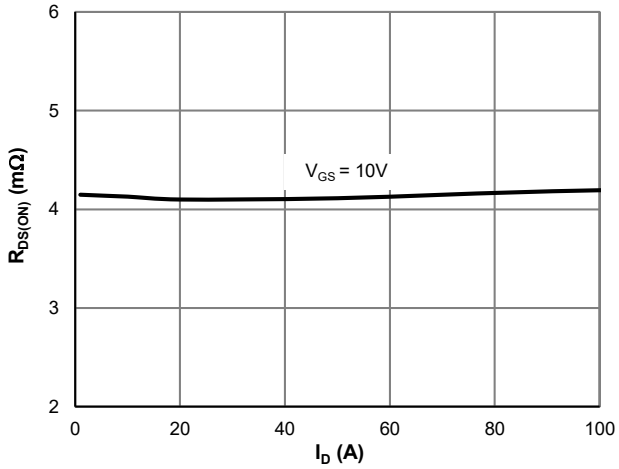


Figure 3: $R_{DS(ON)}$ vs. Drain Current

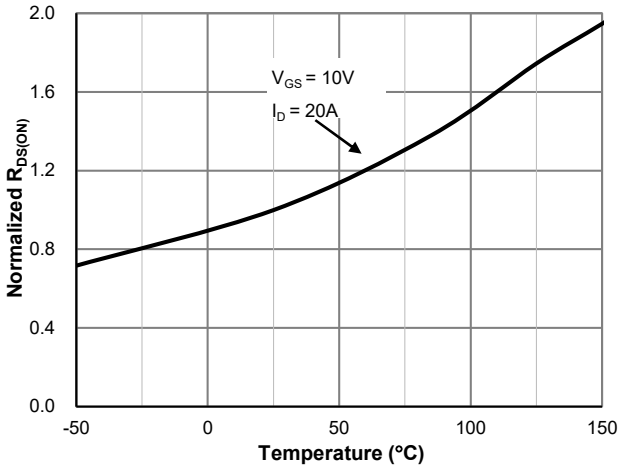


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

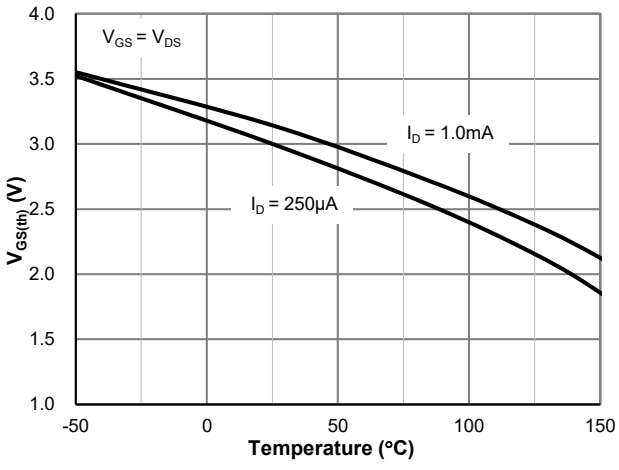


Figure 5: $V_{GS(th)}$ vs. Junction Temperature

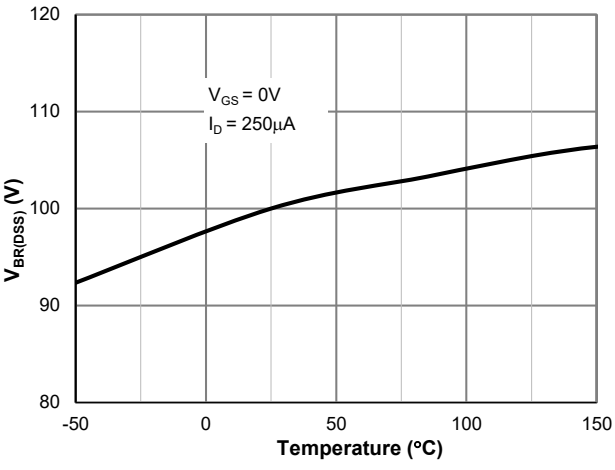


Figure 6: $V_{BR(DSS)}$ vs. Junction Temperature

Typical Characteristics

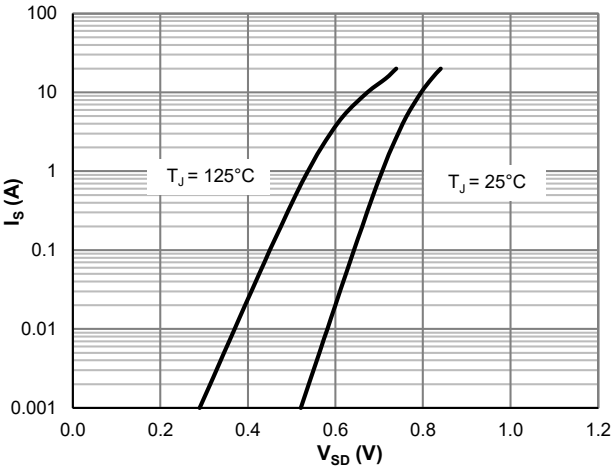


Figure 7: Body-Diode Characteristics

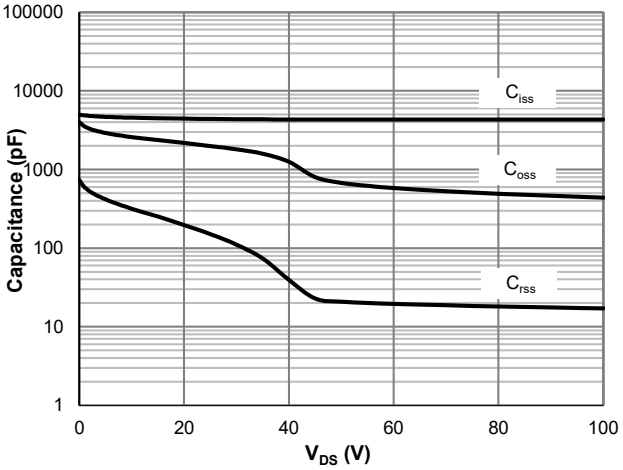


Figure 8: Capacitance Characteristics

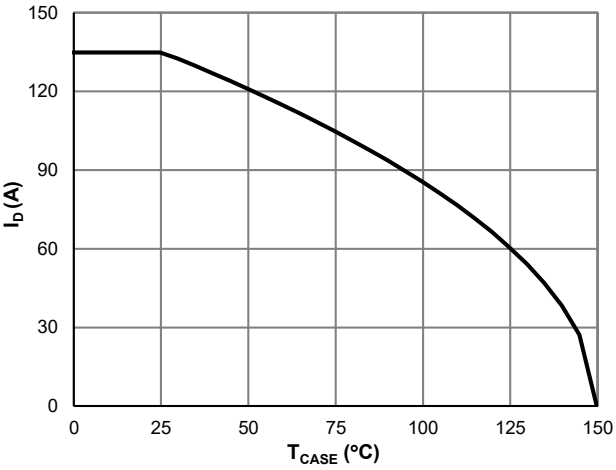


Figure 9: Current De-rating

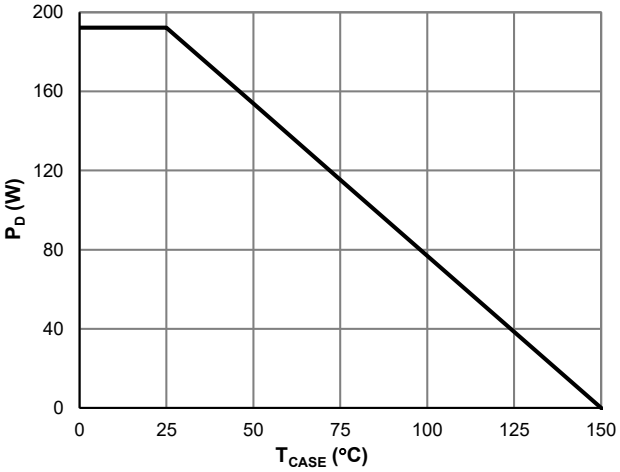


Figure 10: Power De-rating

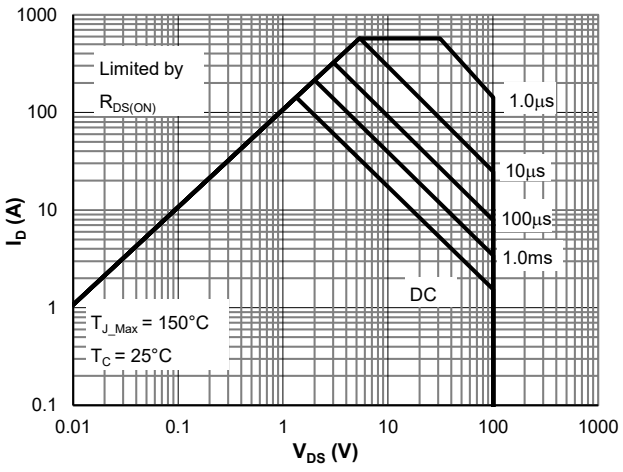


Figure 11: Maximum Safe Operating Area

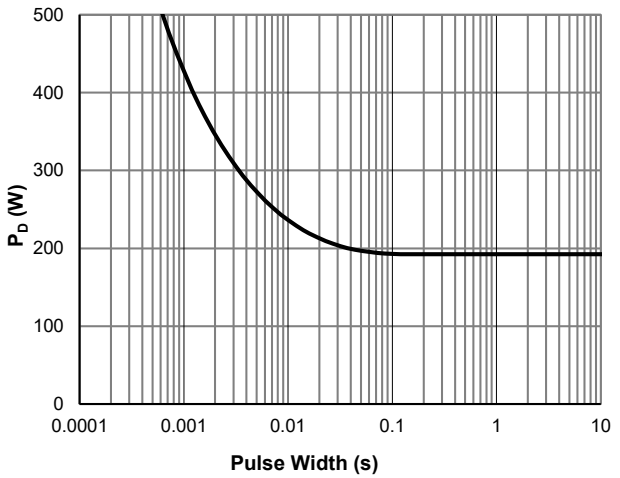


Figure 12: Single Pulse Power Rating, Junction-to-Case

Typical Characteristics

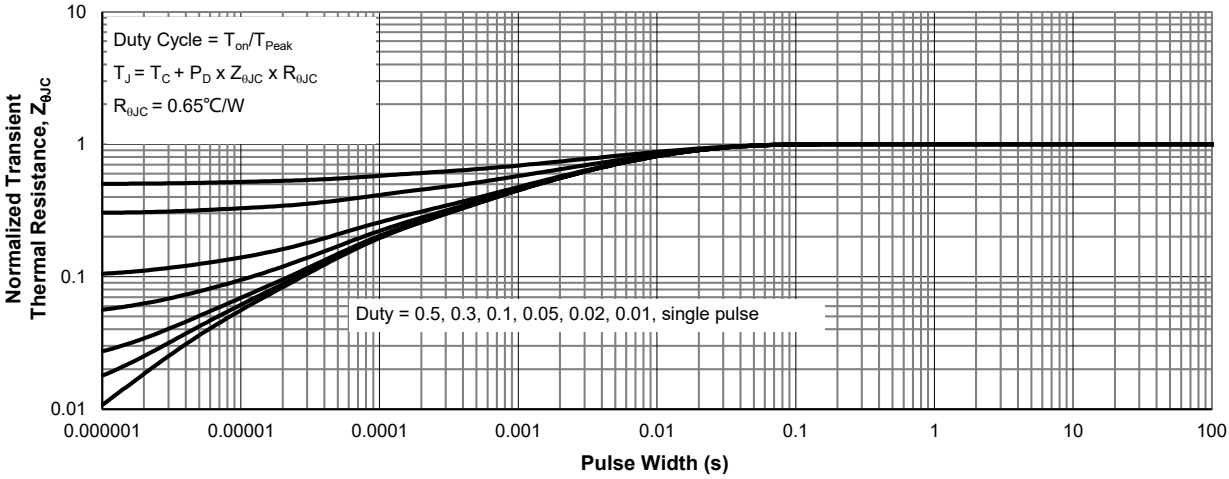
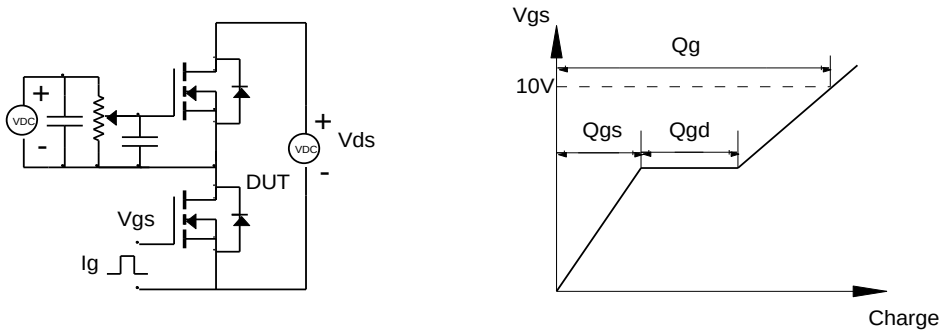


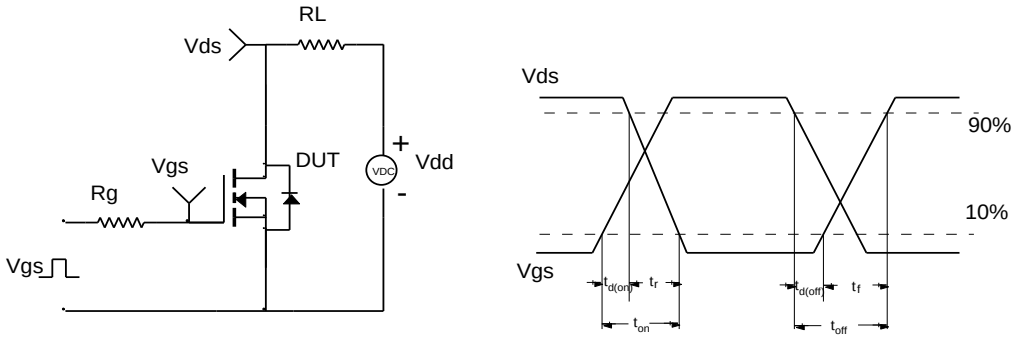
Figure 13: Normalized Maximum Transient Thermal Impedance

Typical Characteristics

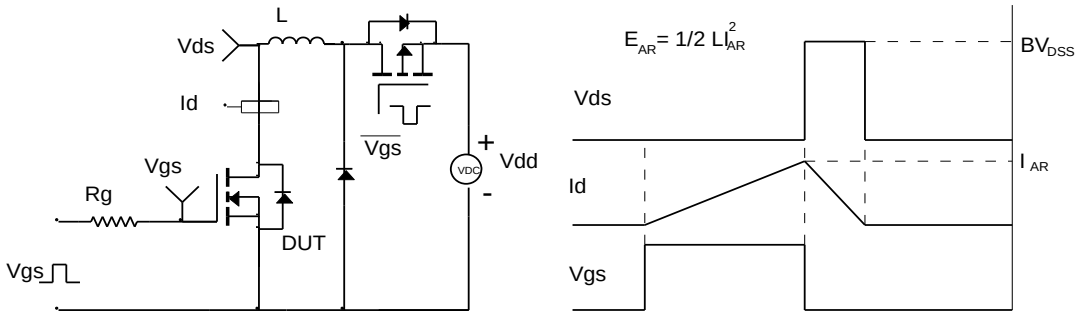
Gate Charge Test Circuit & Waveform



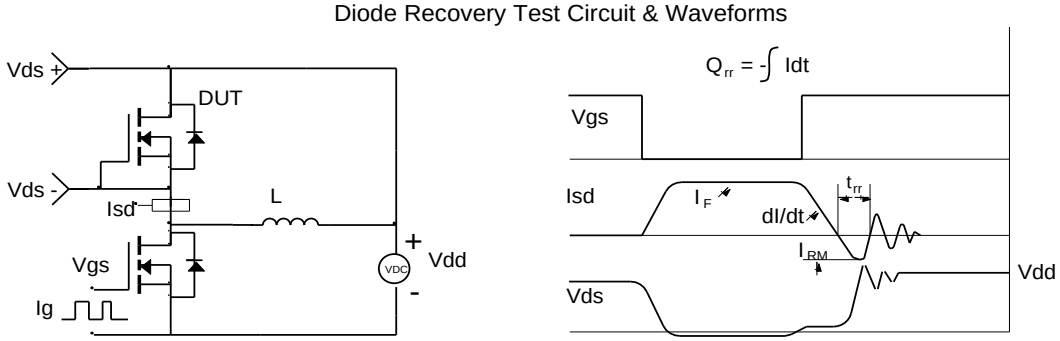
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



TO-220-3L Package Outline Dimensions